WHAT IS CLAIMED IS:

1. An orthogonal code generating circuit for generating an orthogonal code which is defined as a code stream of an Hadamard matrix constructed of $2^k x 2^k$ (symbol "k" being integer larger than, or equal to 0), comprising:

a counter circuit unit for counter-outputting code stream positional signals of said Hadamard matrix from a predetermined initial phase up to a maximum value in an increment order when a code generation starting signal is entered into said counter circuit unit;

a control circuit unit for outputting a decode output based upon a code designation signal used to designate a code number of said Hadamard matrix; and

a combination circuit unit for AND-gating said counter output derived from said counter circuit unit and said decode output derived from said control circuit unit with respect to output bits corresponding thereto, and also for exclusively OR-gating said AND-gated output bits to thereby output serial data of said orthogonal code.

2. An orthogonal code generating circuit as claimed in claim 1 wherein:

said control circuit unit outputs said decode output after plural bits of said code designation signal defined from an upper-grade bit up to a down-grade bit are replaced with each other; and

said combination circuit unit outputs an orthogonal code which is defined by said decode output as a code stream of a hierarchical orthogonal code.

3. An orthogonal code generating circuit as claimed in claim 1 wherein:

said control circuit unit outputs said decode output in such a manner that since a code length designation signal for designating a code length shorter than, or equal to a maximum code length is inputted, said code designation signal is used so as to designate a code length designated based upon said code length designation signal; and

said combination circuit unit outputs said orthogonal code made based upon said code designation signal for the designated code length.

4. An orthogonal code generating circuit as claimed in claim 1 wherein:

said counter circuit unit starts said counter output from said initial phase when a code initial phase setting value is entered, said initial phase corresponding to said code initial phase setting value.

5. An orthogonal code generating circuit as claimed in claim 2 wherein:

said control circuit unit switches said orthogonal code related to either said Hadamard matrix or said hierarchical orthogonal code when a code generation switching signal is entered.

6. An orthogonal code generating circuit as claimed in any one of Claims 1 to 5, wherein said orthogonal code generating circuit is used for a demodulating process apparatus.

7. An orthogonal code generating circuit as claimed in any one of Claims

1 to 5, wherein said orthogonal code generating circuit is used for a synchronizing process apparatus.

8. An orthogonal code generating circuit as claimed in any one of Claims 1 to 5, wherein said orthogonal code generating circuit is used for a spreading process apparatus.

9. An orthogonal code generating circuit as claimed in Claim 6, wherein, said demodulating process apparatusis used for a reception apparatus of a spectrum spread signal.

10. An orthogonal code generating circuit as claimed in Claim 7, wherein, said synchronizing process apparatus is used for a reception apparatus of a spectrum spread signal.

11. An orthogonal code generating circuit as claimed in Claim 8, wherein, said spreading process apparatus is used for a transmission apparatus of a spectrum spread signal.

12. An orthogonal code generating circuit as claimed in any one of Claims 1 to 5, wherein said orthogonal code generating circuit is used for a base station apparatus comprising at least any one of a demodulating process apparatus, a synchronizing process apparatus, and a spreading process apparatus.

13. An orthogonal code generating circuit as claimed in any one of Claims

1 to 5, wherein said orthogonal code generating circuit is used for a mobile terminal apparatus comprising at least any one of a demodulating process apparatus, a synchronizing process apparatus, and a spreading process apparatus.

14. An orthogonal code generating circuit as claimed in any one of Claims 1 to 5, wherein said orthogonal code generating circuit is used for a mobile communication system which is comprised of a mobile terminal apparatus and a base station, in which at least any one of a demodulating process apparatus, a synchronizing process apparatus, and a spreading process apparatus is provided.